

ARTIX-7 FPGA
Development Board

AX7A035B

User Manual

REV 1.1

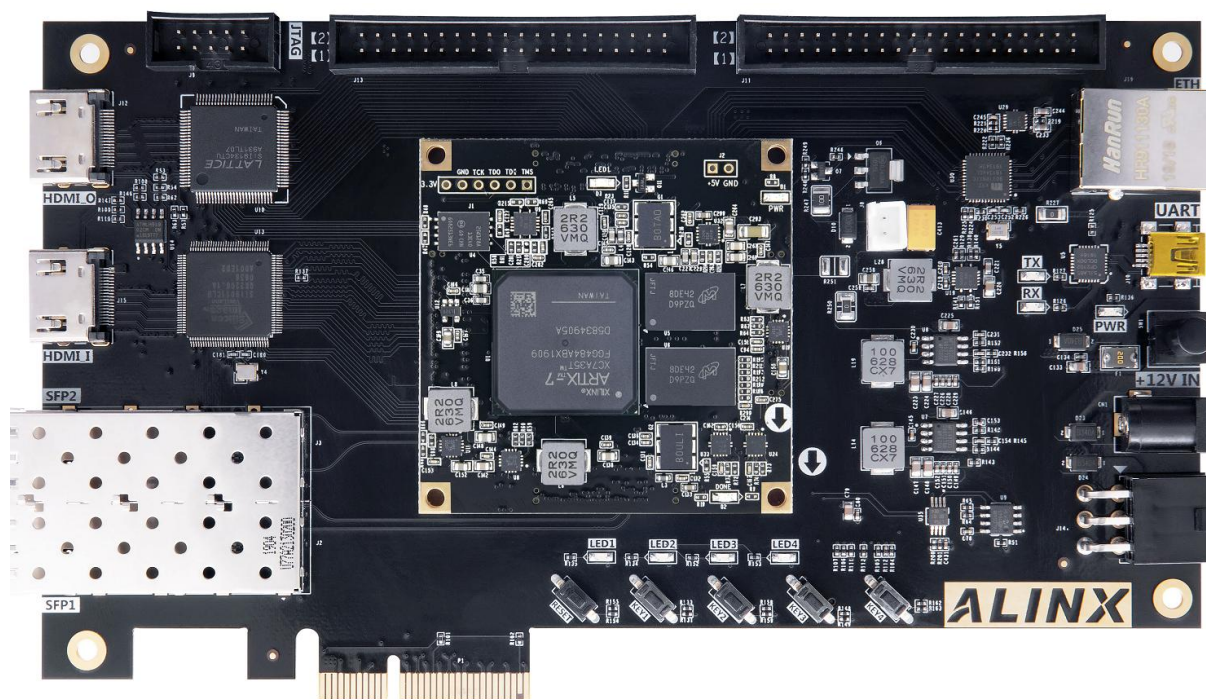


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This ARTIX-7 FPGA development platform (Module: AX7A035B) adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 PCIe2 interface, 2 SFP module interfaces, 1 HDMI output interface, 1 HDMI input interface, 1 Gigabit Ethernet interface, Uart Interface, SD card slot etc. It meets user's requirements for PCIe high-speed data exchange, video transmission processing and industrial control. It is a "Versatile" ARTIX-7 FPGA development platform. It provides the possibility for high-speed video transmission, pre-validation and post-application of network, fiber and PCIe communication and data processing. This product is very suitable for students, engineers and other groups engaged in ARTIX-7 FPGA development.



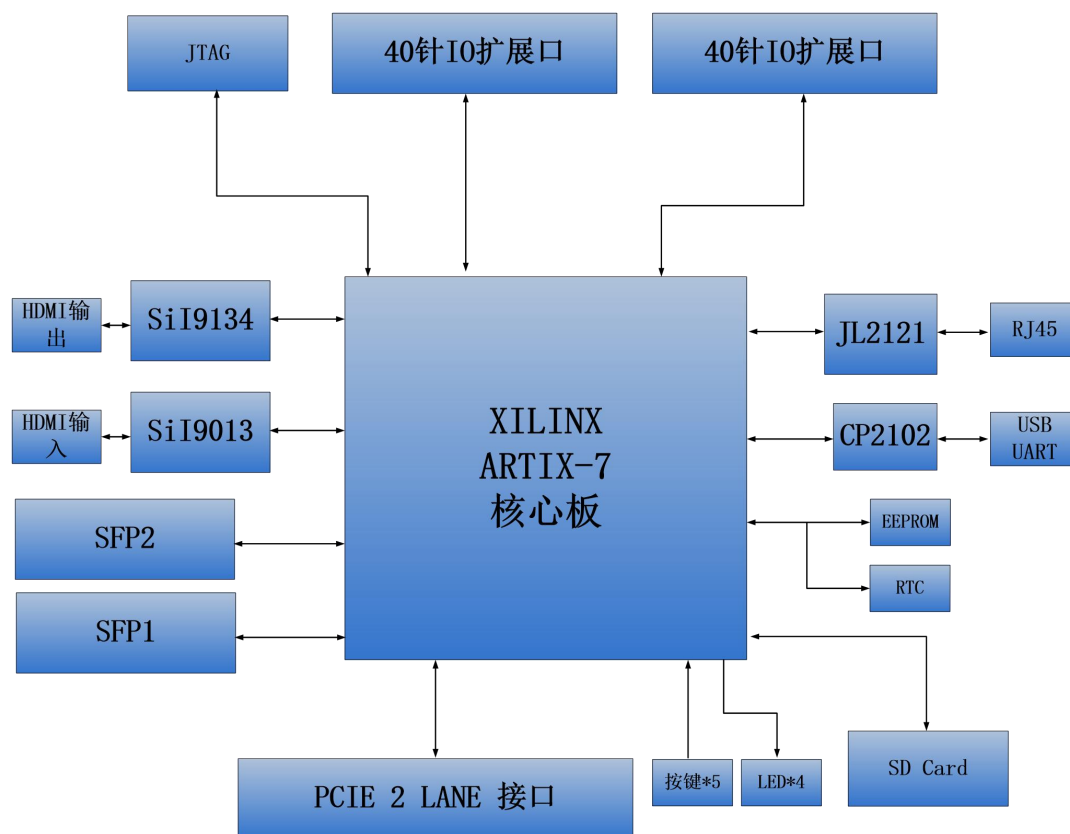
1. FPGA Development Board Introduction

The entire structure of the AX7A035B FPGA development board is inherited from our consistent core board+carrier board model. High-speed inter-board connectors are used between the core board and the carrier board.

The core board is mainly composed of FPGA + 2 DDR3 + QSPI FLASH, which undertakes the functions of high-speed data processing and storage of FPGA, high-speed data reading and writing between FPGA and two DDR3s, data bit width is 32 bits, and the bandwidth of the whole system is up to 25Gb/s (800M*32bit); The two DDR3 capacities are up to 8Gbit, which meets the need for high buffers during data processing. The selected FPGA is the XC7A35T chip of XILINX's ARTIX-7 series, in BGA 484 package. The communication frequency between the XC7A35T and DDR3 reaches 400Mhz and the data rate is 800Mhz, which fully meets the needs of high-speed multi-channel data processing. In addition, the XC7A35T FPGA features four GTP high-speed transceivers with speeds up to 6.6Gb/s per channel, making it ideal for fiber-optic communications and PCIe data communications.

The AX7A035B carrier board expands rich peripheral interfaces for core board, including 1 PCIe x2 interface, 2 SFP Interfaces, 1 HDMI output interface, 1 HDMI input interface, 1 Uart interface, 1 Gigabit Ethernet interface, 1 SD card interface, 2 40-pin expansion ports, some Keys, LED and EEPROM circuit.

The following is the structure diagram of the whole development system:



Through this diagram, you can see the interfaces and functions that the AX7A035B FPGA Development Board contains:

- Artix-7 FPGA core board

The core board consists of XC7A35T + 8Gb DDR3 + 128Mb QSPI FLASH. There are two high-precision Sitime LVDS differential crystals, one at 200MHz and the other at 125MHz, providing stable clock input for FPGA systems and GTP modules.

- 1-channel PCIe x2 interface

Supports PCI Express 2.0 standard, provides PCIe x 2 high-speed data transmission interface, single channel communication rate up to 5Gbaud.

- 2-channel high-speed SFP Interfaces

The two high-speed transceivers of the GTP transceiver of ARTIX-7 FPGA are connected to the transmission and reception of two optical modules to realize two high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds up to 6.6 Gb/s.

- 1-channel 10/100M/1000M Ethernet RJ-45 interface

Gigabit Ethernet interface chip adopts JL2121 industrial-grade GPHY chip of JLSemi company. The JL2121 chip supports 10/100/1000 Mbps network transmission rate; supports Full duplex and self-adaptive.

- 1-channel HDMI Output interface

Silion Image's SIL9134 HDMI encoding chip is selected to support up to 1080P@60Hz output and support 3D output.

- 1-channel HDMI Input interface

Silion Image's SIL9011/ SIL9013 HDMI decoding chip is selected to support up to 1080P@60Hz input and support data output in different formats.

- 1-channel USB-to-Uart interface

1-channel USB-to-Uart interface for communication with the computer for user debugging. The serial port chip is the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is the MINI USB interface.

- Micro SD card holder

1-channel Micro SD card slot, support SD mode and SPI mode.

- EEPROM

An IIC interface EEPROM 24LC04 on board.

- 2-channel 40-pin expansion ports

Reserve 2-channel 40-pin 0.1 inch pitch expansion ports, which can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains one 5V power supply, two 3.3V power supplies, three ground supplies, 34 IO ports.

- JTAG Interface

A 10-pin 0.1 inch spacing standard JTAG interface for FPGA program downloading and debugging.

- Keys

4 keys; 1 reset key (on the core board)

- LED Light

5 user LEDs (1 on the core board and 4 on the carrier board)

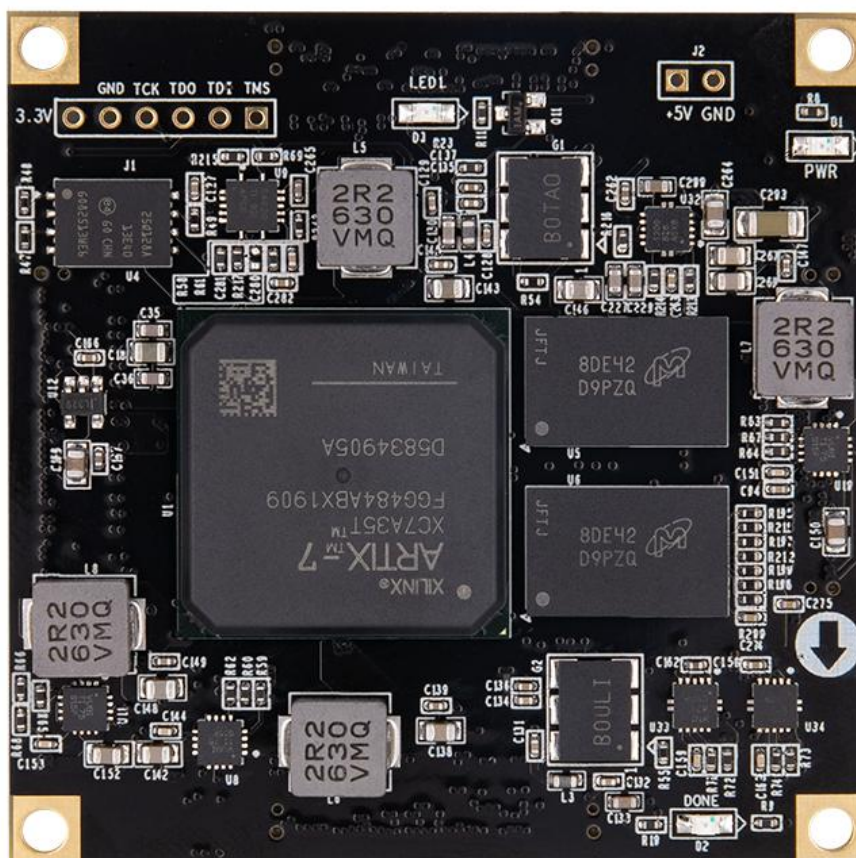
2. FPGA Core Board

2.1 Introduction

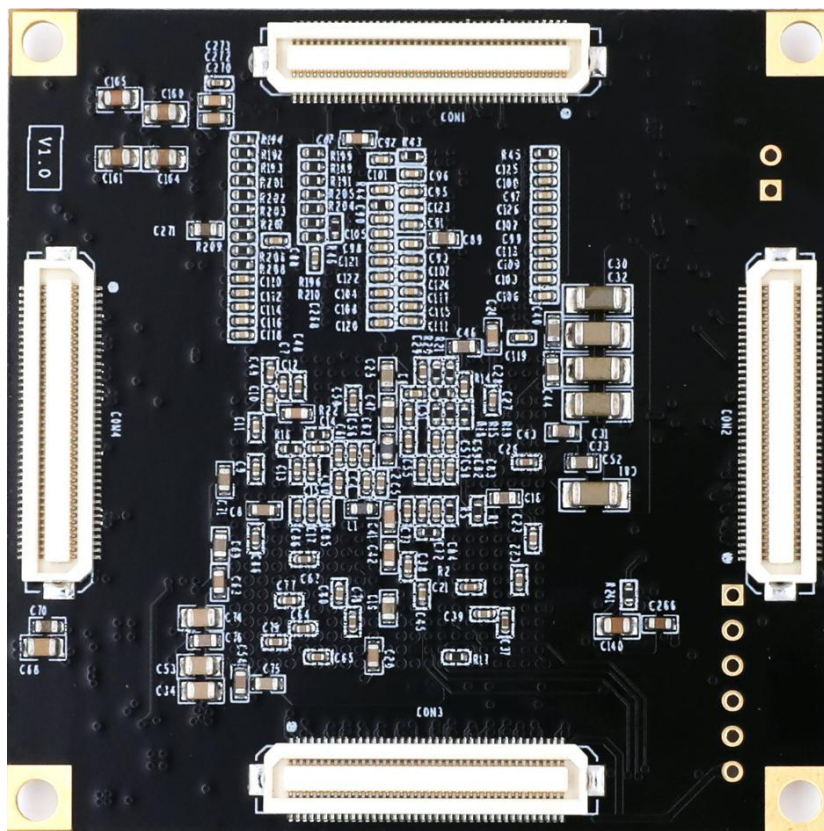
AC7A035 (core board model, the same below) FPGA core board is based on XILINX's ARTIX-7 series 100T XC7A35T-2FGG484I, which is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition etc.

AC7A035 core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chips, each DDR has a capacity of 4Gbit; two DDR chips are combined into a 32-bit data bus width, and the read/write data bandwidth between FPGA and DDR3 is up to 25Gb; such a configuration can meet the needs of high bandwidth data processing.

The AC7A035 core board expands 146 standard IO ports with 3.3V level, 15 standard IO ports with 1.5V level, and 4 pairs of GTP high speed RX/TX differential signals. For users who need a lot of IOs, this core board will be a good choice. Moreover, lines between the FPGA chip and interfaces are processed with equal length and differential length, and the core board size is only 2.36 inch *2.36 inch, which is very suitable for secondary development.



AC7A035 Front View



AC7A035 Back View

2.2 FPGA

As mentioned above, the FPGA model we use is XC7A35T-2FGG484I, which belongs to Xilinx's Artix-7 series. The speed grade is 2, and the temperature grade is industrial grade. This model is a FGG484 package with 484 pins. Xilinx ARTIX-7 FPGA chip naming rules as below:

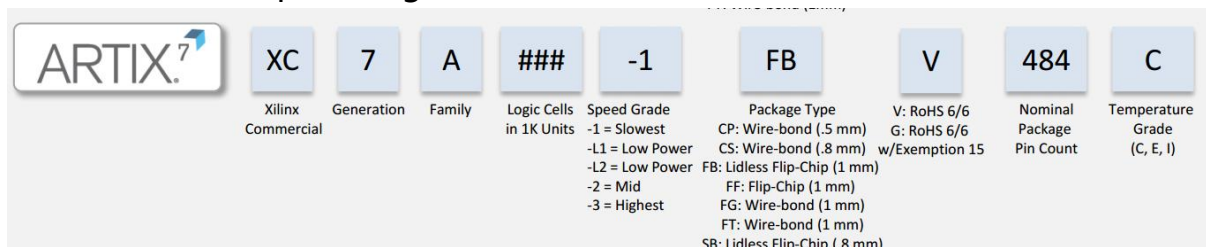


Figure 2-2-1 shows the FPGA chip used on development board:



Figure 2-2-1 FPGA chip

The main parameters of the FPGA chip XC7A35T are as follows:

Name	Parameters
Logic Cells	33,280
Slices	5,200
CLB flip-flops	41,600
Block RAM (kb)	1,800
DSP Slices	90
PCIe Gen2	1
XADC	1 XADC, 12bit, 1Mbps AD
GTP Transceiver	4 ↑, 6.6Gb/s max
Speed grade	-2

Temperature Grade	Industrial
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FPGA power supply system

Artix-7 FPGA power supplies are V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCO} , $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the power supply pin for the FPGA kernel and needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA Block RAM, connected to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, connected to 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK13~16, BANK34~35. On AC7A035 FPGA core board, because BANK34 and BANK35 need to be connected to DDR3, their voltage connect to 1.5V, and the voltage of other BANK is 3.3V. The V_{CCO} of BANK15 and BANK16 is powered by the LDO, and the level of BANK can be changed by replacing the LDO chip. $V_{MGTAVCC}$ is the supply voltage of the FPGA internal GTP transceiver, connected to 1.0V; $V_{MGTAVTT}$ is the termination voltage of the GTP transceiver, connected to 1.2V.

The Artix-7 FPGA system requires that the power-up sequence should be $V_{CCINT} \rightarrow V_{CCBRAM} \rightarrow V_{CCAUX} \rightarrow V_{CCO}$. If V_{CCINT} and V_{CCBRAM} have the same voltage, they can be powered up at the same time. The order of power-off sequence is reversed. The power-up sequence of the GTP transceiver is $V_{CCINT} \rightarrow V_{MGTAVCC} \rightarrow V_{MGTAVTT}$. If V_{CCINT} and $V_{MGTAVCC}$ have the same voltage, they can be powered up at the same time. The power-off sequence is just reversed.

2.3 Active Differential Crystal

The AC7A035 core board is equipped with two Sitime active differential crystals, one is 200MHz, model SiT9102-200.00MHz, used for the system master clock of FPGA and for generating DDR3 control clock; the other is 125MHz, model SiT9102-125MHz, used for reference clock input of GTP transceivers.

2.3.1 200Mhz Differential clock

G1 in Figure 2-3-1 is the 200M active differential crystal oscillator circuit, that is the system clock source provided for the development board mentioned above. The crystal output is connected to the BANK34 global clock pin MRCC (R4 and T4) of the FPGA. This 200Mhz differential clock can be used to drive the user logic in the FPGA. Users can configure the PLLs and DCMs inside the FPGA

to generate clocks with different frequencies.

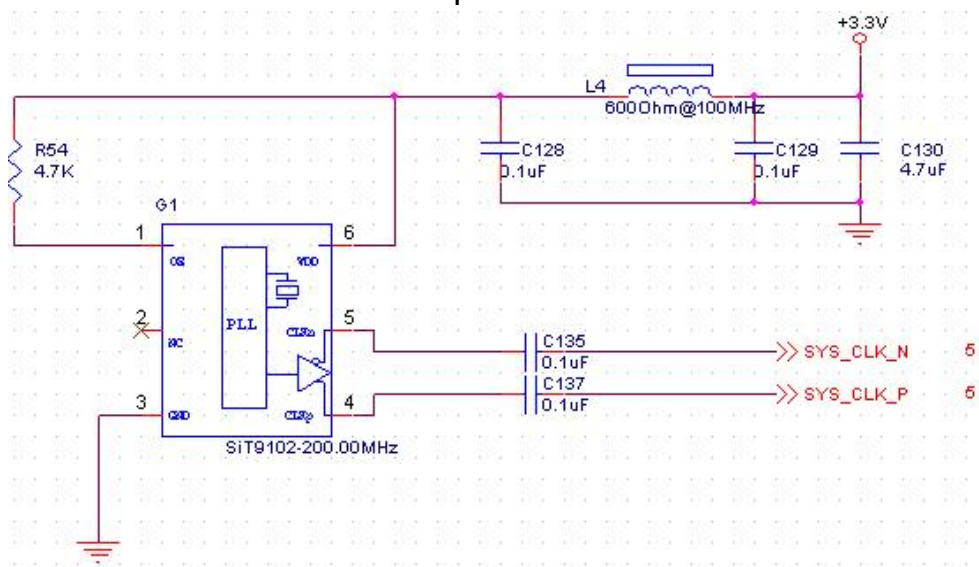


Figure 2-3-1: 200Mhz Active Differential Crystal Schematic

200Mhz Differential Clock Pin Assignment:

Pin Name	FPGA Pin
SYS_CLK_P	R4
SYS_CLK_N	T4

2.3.2 125Mhz Differential Crystal

G2 in Figure 2-3-2 is the 125M active differential crystal oscillator circuit. This clock is the reference input clock for the GTP module inside the FPGA. The crystal output is connected to the GTP BANK216 clock pins MGTREFCLK0P (F6) and MGTREFCLK0N (E6) of the FPGA.

GTP CLOCK

125MHz

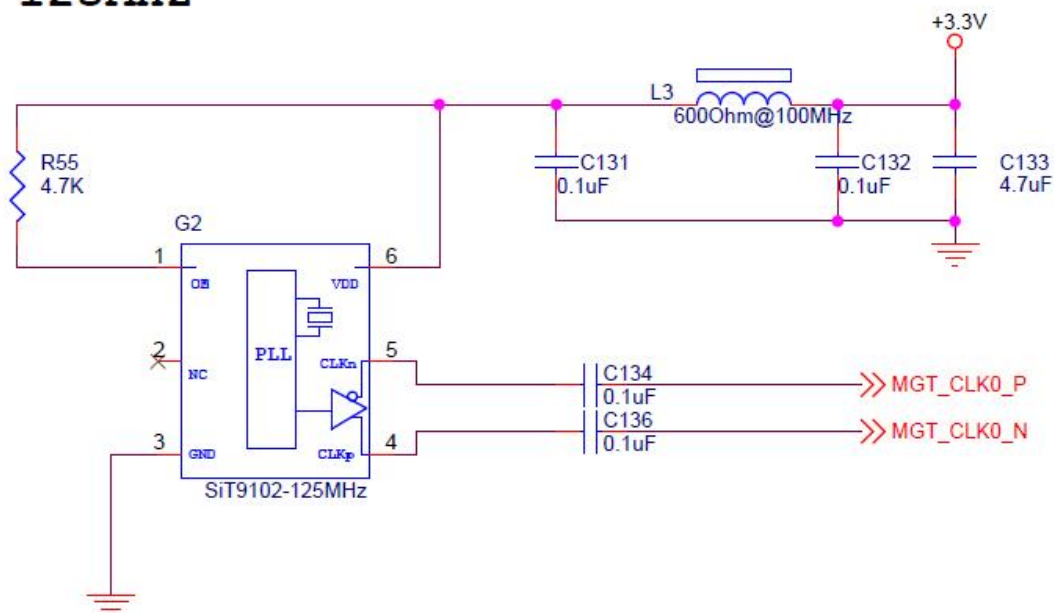


Figure 2-3-2: 125MHz Active Differential Crystal Schematic

125MHz Differential Clock Pin Assignment:

Pin Name	FPGA Pin
MGT_CLK0_P	F6
MGT_CLK0_N	E6

2.4 DDR3

The FPGA core board AC7A035 is equipped with two Micron 4Gbit (512MB) DDR3 chips (8Gbit in total), model MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The total bus width of DDR is 32bit. The DDR3 SDRAM has a maximum operating clock speed of 400MHz (data rate of 800Mbps). The DDR3 memory system is directly connected to the memory interface of the FPGA's BANK 34 and BANK35. Table 2-4-1 shows the DDR3 SDRAM configuration.

Table 2-4-1: DDR3 SDRAM Configuration

Bit Number	Chip Model	Capacity	Manufacturer
U5,U6	MT41J256M16HA-125	256M x 16bit	micron

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, line impedance control, and line length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3. Figure 2-4-1 shows the hardware connection of DDR3 DRAM.

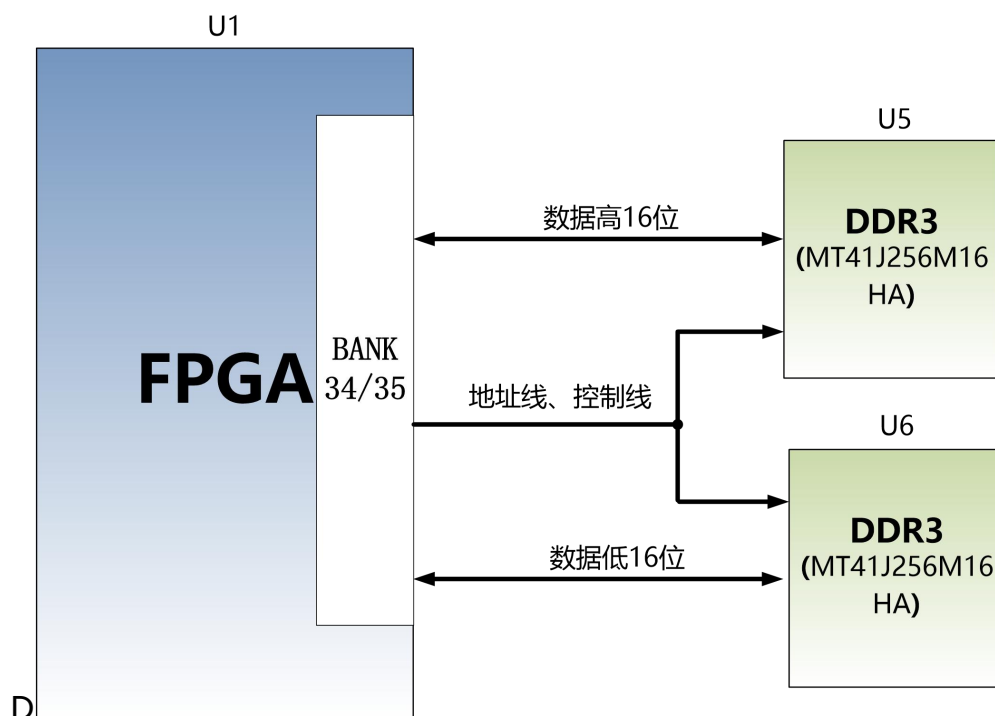


Figure 2-4-1: The DDR3 DRAM Schematic

DDR3 DRAM pin assignment:

Signal Name	FPGA Pin Name	FPGA Pin Number
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1

DDR3_DQ [3]	IO_L6P_T0_35	F3
DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2

DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3
DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2
DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1
DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3
DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

2.5 QSPI Flash

The FPGA core board AC7A035 is equipped with one 128Mbit QSPI FLASH, model N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, soft core application code and other user data files. Table 2-5-1 shows the specific models and related parameters of SPI FLASH.

Bit Number	Model	Capacity	Manufacturer
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1: QSPI FLASH model and parameter

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip-selected signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 2-5-1 shows the hardware connection of QSPI Flash.

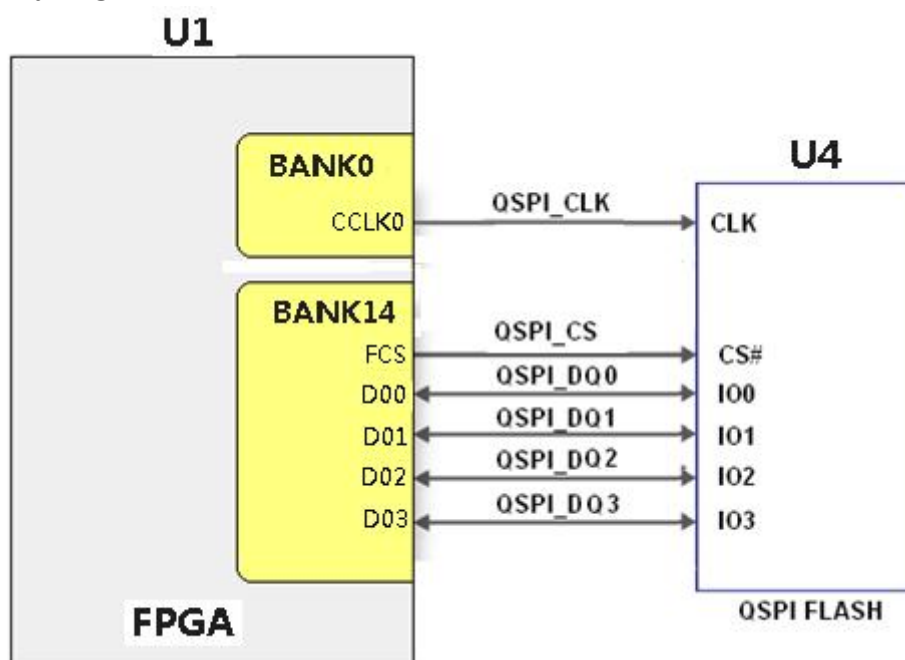


Figure 2-5-1 QSPI Flash connection diagram

QSPI Flash pin assignment:

Signal Name	FPGA Pin Name	FPGA Pin Number
QSPI_CLK	CCLK_0	L12

QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

2.6 LED

There are 3 red LED lights on the AC7A035 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light (LED1). When the core board is powered, the power indicator will light up; when the FPGA is configured, the configuration LED will light up. The user LED light is connected to the IO of the BANK34, then users can control the light on and off through the program. When the IO voltage connected to the user LED is high, the user LED is light up. When the connection IO voltage is low, the user LED will light off. Figure 2-6-1 shows the schematic diagram of the LED light hardware connection:

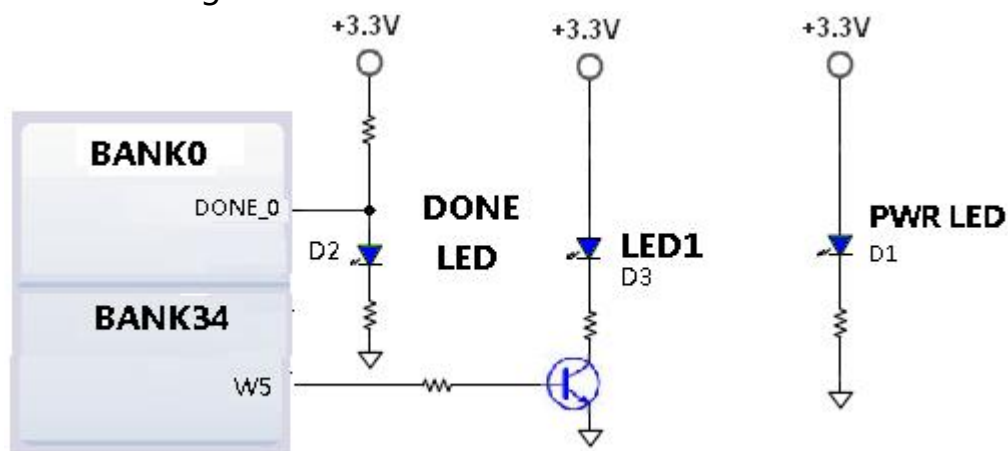


Figure 2-6-1 LED light hardware connection

User LED Pin Assignment:

Signal Name	FPGA Pin Name	FPGA Pin Number	Description
LED1	IO_L15N_T2_DQS_34	W5	User LED

2.7 JTAG Interface

The JTAG test socket J1 is reserved on the AC7A035 core board for JTAG downloading and debugging when the core board is used alone. Figure 2-7-1 shows the schematic of the JTAG interface, which involves six signals including TMS,TDI,TD0,TCK,GND and +3.3V.

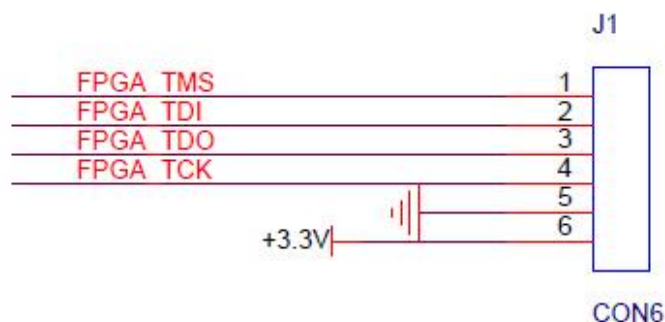


Figure 2-7-1: JTAG Interface Schematic

JTAG interface J1 on the core board adopts 6-pin 2.54mm pitch single-row test holes. If users need to use JTAG connection and debugging on the core board, 6-pin single-row pin headers need to be welded.

2.8 Power Interface

In order to make the AC7A035 FPGA core board work independently, the core board is reserved 2-pin power supply interface J2. If the user wants to debug the function of the core board separately (without the carrier board), +5V power needed to be externally supplied to the core board.

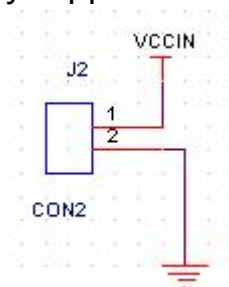


Figure 2-8-1: Power Interface circuit

2.9 Board to Board Connectors

A total of four high-speed expansion ports are extended on the back of the core board, using four 80-Pin board-to-board connectors to connect to the carrier board. Connectors use Panasonic AXK580137YG, and connectors corresponded on the carrier board is AXK680337YG. The IO ports of the FPGA are connected to the four expansion ports through differential lining. The PIN spacing of connectors is 0.5mm, configuring with female connectors on the carrier board to realize high-speed data communication.

Connector CON1

The 80-Pin connector CON1 is used to connect the VCCIN power supply (+5V) of the carrier board, the ground, and the normal IO of the FPGA. It should be noted here that 15 pins of the CON1 are connected to the IO port of the BANK34, because the BANK34 is connected to the DDR3, therefore, the voltage standard of all IOs of this BANK34 is 1.5V. **In addition, the XC7A35T chip does not have BANK13, so the IO of BANK13 cannot be used for the AX7A035B development board.**

Pin Assignment of Board to Board Connector CON1:

CON1 Pin	Signal Name	FPGA Pin No.	Level	CON1 Pin	Signal Name	FPGA Pin No.	Level
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	NC	-	NC	PIN12	NC	-	NC
PIN13	NC	-	NC	PIN14	NC	-	NC
PIN15	NC	-	NC	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	NC	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V

PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_N	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	XADC_VN	M9	Analog	PIN52	NC		
PIN53	XADC_VP	L10	Analog	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	NC	PIN56	B34_L24_P	W9	1.5V
PIN57	NC	-	NC	PIN58	B34_L24_N	Y9	1.5V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	NC
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	NC
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	NC
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	NC
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	NC
PIN73	B16_L6_P	D14	3.3V	PIN74	NC	-	NC
PIN75	B16_L8_P	C13	3.3V	PIN76	NC	-	NC
PIN77	B16_L8_N	B13	3.3V	PIN78	NC	-	NC
PIN79	NC	-	NC	PIN80	NC	-	NC

Connector CON2

The 80-pin connector CON2 is used to extend the normal IO of the FPGA

BANK13 and BANK14, both of which have a 3.3V voltage standard. In addition, the XC7A35T chip does not have BANK13, so the IO of BANK13 cannot be used for the AX7A035B development board.

Pin Assignment of Board to Board Connector CON2:

CON2 Pin	Signal Name	FPGA Pin No.	Level	CON2 Pin	Signal Name	FPGA Pin No.	Level
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V
PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V
PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V
PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V
PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND

PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V

Connector CON3

The 80-pin connector CON3 is used to extend the normal IO of the BANK15 and BANK16, and four JTAG signals are also connected to the carrier board through the CON3 connector. BANK15 and BANK16 voltage standards can be adjusted by an LDO chip, the default installed LDO is 3.3V, if users want to output other standard levels, they can replace appropriate LDO to achieve.

Pin Assignment of Board to Board Connector CON3:

CON3 Pin	Signal Name	FPGA Pin No.	Level	CON3 Pin	Signal Name	FPGA Pin No.	Level
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V

PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V
PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V
PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V
PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V
PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	

PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

Connector CON4

The 80-pin connector CON4 is used to extend the normal IO of FPGA BANK16 and high-speed data and clock signals of GTP. The voltage standard of BANK16 IO ports can be adjusted by LDO chip. The default LDO installed is 3.3V. If users want to output other standard levels, they can replace appropriate LDO to achieve this. The high-speed data and clock signal of GTP are strictly differentiated on the core board, and the data lines are equal in length and maintained at a certain interval to prevent signal interference.

Pin Assignment of Board to Board Connector CON4:

CON4 Pin	Signal Name	FPGA Pin No.	Level	CON4 Pin	Signal Name	FPGA Pin No.	Level
PIN1	NC		NC	NC		NC	NC
PIN3	NC		NC	NC		NC	NC
PIN5	NC		NC	NC		NC	NC
PIN7	NC		NC	NC		NC	NC
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	NC		NC	PIN12	MGT_TX2_P	B6	Diff
PIN13	NC		NC	PIN14	MGT_TX2_N	A6	Diff
PIN15	GND	-	GND	PIN16	GND	-	GND
PIN17	MGT_TX3_P	D7	Diff	PIN18	MGT_RX2_P	B10	Diff
PIN19	MGT_TX3_N	C7	Diff	PIN20	MGT_RX2_N	A10	Diff
PIN21	GND	-	GND	PIN22	GND	-	GND
PIN23	MGT_RX3_P	D9	Diff	PIN24	MGT_TX0_P	B4	Diff
PIN25	MGT_RX3_N	C9	Diff	PIN26	MGT_TX0_N	A4	Diff
PIN27	GND	-	GND	PIN28	GND	-	GND
PIN29	MGT_TX1_P	D5	Diff	PIN30	MGT_RX0_P	B8	Diff
PIN31	MGT_TX1_N	C5	Diff	PIN32	MGT_RX0_N	A8	Diff
PIN33	GND	-	GND	PIN34	GND	-	GND

PIN35	MGT_RX1_P	D11	Diff	PIN36	MGT_CLK1_P	F10	Diff
PIN37	MGT_RX1_N	C11	Diff	PIN38	MGT_CLK1_N	E10	Diff
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V
PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V
PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V
PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V
PIN79	NC	-		PIN80	NC	-	

2.10 Power Supply

The power supply voltage of the AC7A035 core board is DC5V. When the AC7A035 core board is used separately, it supplies power through the J2 interface. When the AC7A035 core board is connected to the carrier board, it supplies power through the carrier board. Please be careful not use J2 and carrier board to supply power at the same time to avoid damage. Figure 2-10-1 shows the power supply design diagram on the board:

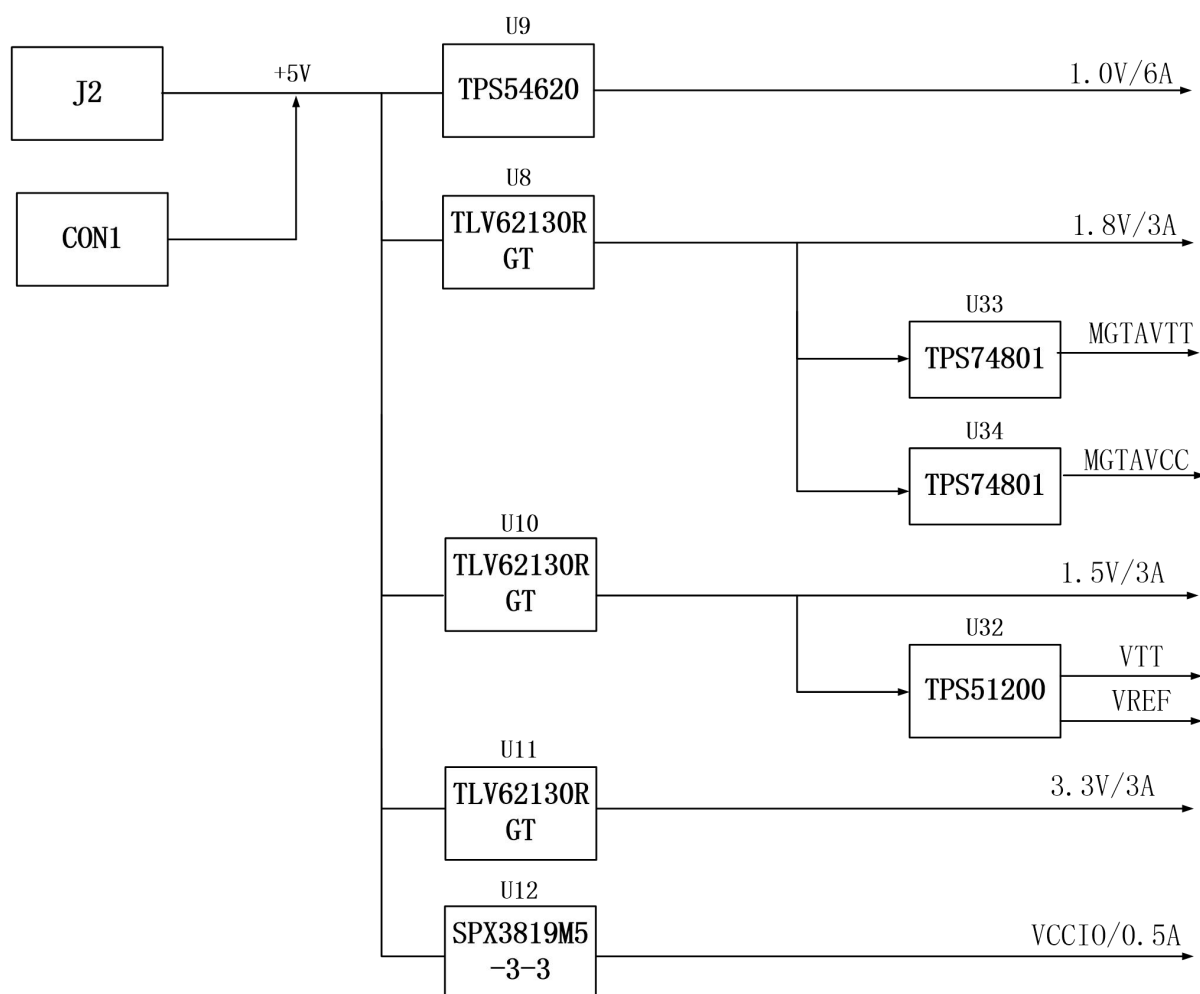


Figure 2-10-1: Power Supply on core board

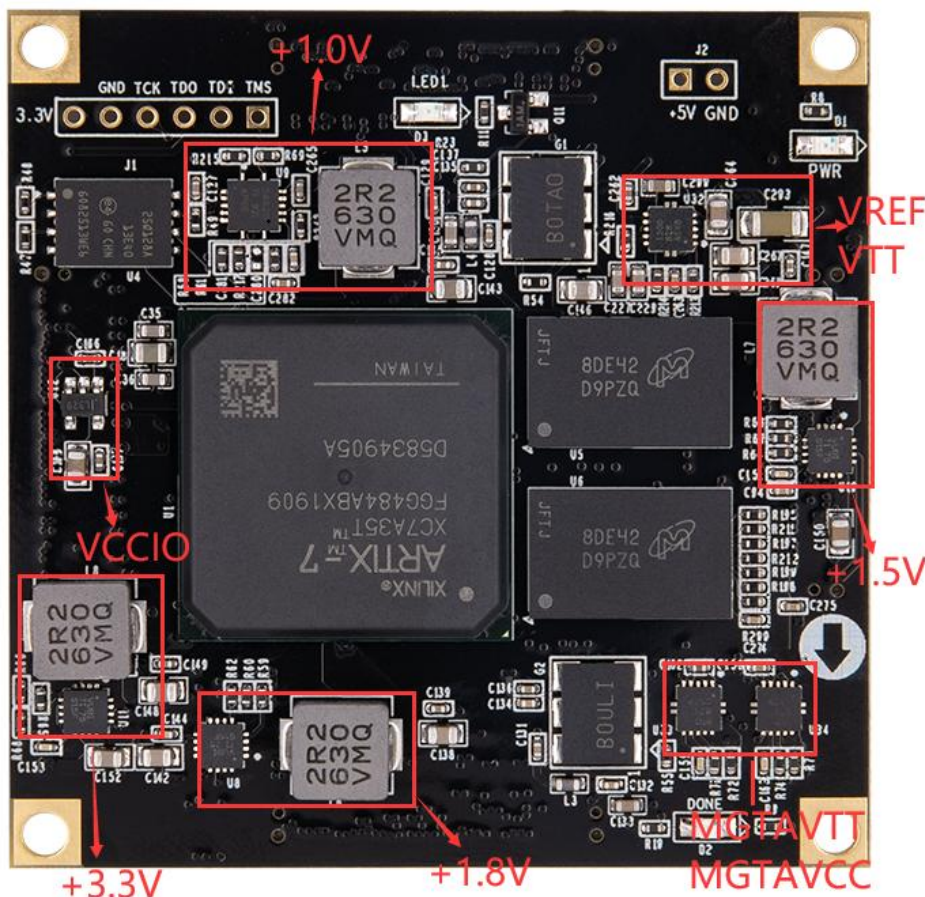
The core board is powered by +5V, and converted into +3.3V, +1.5V, +1.8V, +1.0V power supplies through the 3-channel DC/DC power supply chip TLV62130RGT and TPS54620, in which the current of +1.0V can be up to 6A and the output current of the other 3 power supplies can be up to 3A. In addition, through one LDO SPX3819M5-3-3 to generate VCCIO power supply, VCCIO is mainly used to supply power to FPGA BANK15 and BANK16. Users can replace other LDO chips to make the IO of BANK15 and BANK16 adapts to different voltage standards. 1.5V generates the VTT and VREF voltage required for DDR3 through TI's TPS51200. The 1.8V generates the power supply MGTAVTT and MGTAVCC for the GTP transceiver through TI's TPS74801 chip. The functions of each power distribution are shown in the following table:

Power Supply	Function
+3.3V	FPGA Bank0, Bank13, Bank14 VCCIO,

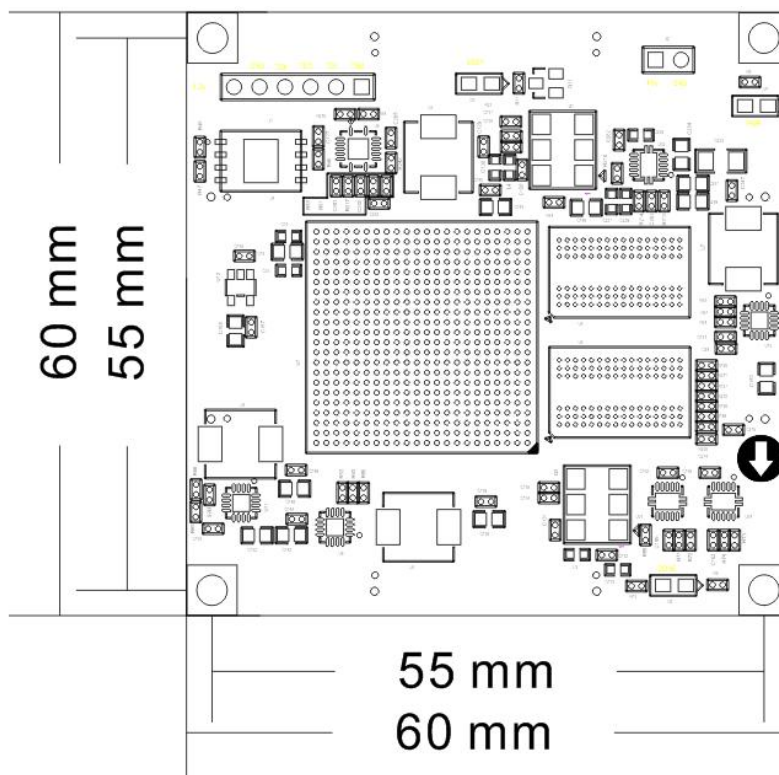
	QSIP FLASH, Clock crystal oscillator
+1.8V	FPGA auxiliary voltage, TPS74801 power supply
+1.0V	The core voltage of the FPGA
+1.5V	DDR3, FPGA Bank34 and Bank35
VREF, VTT (+0.75V)	DDR3
VCCIO(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	FPGA GTP transceiver Bank216
MGTAVCC(+1.0V)	FPGA GTP transceiver Bank216

Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is 1.0V->1.8V->(1.5 V, 3.3V, VCCIO) and 1.0V-> MGTAVCC -> MGTAVTT, the circuit design to ensure the normal operation of the chip.

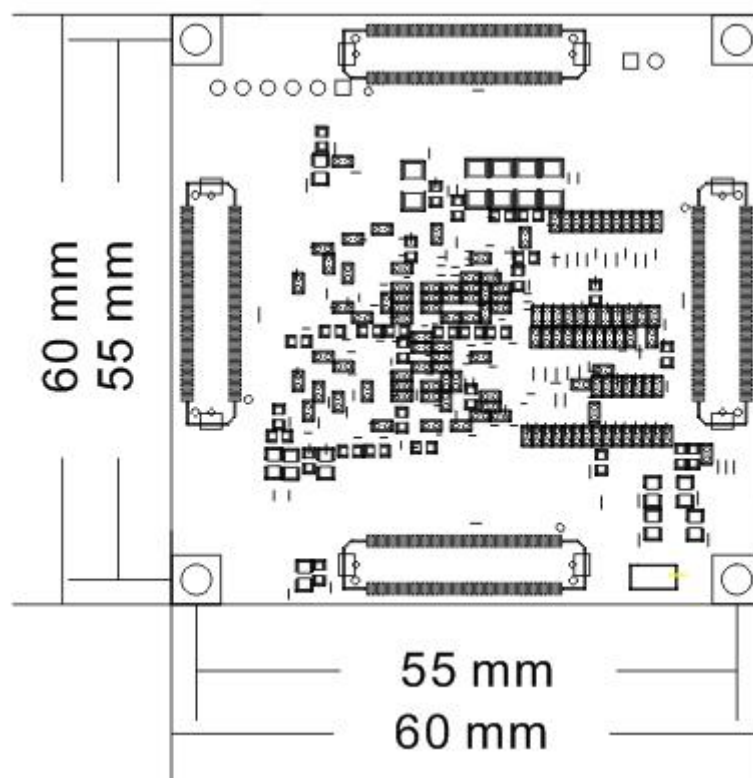
The power circuit on the AC7A035 FPGA core board is shown in Figure 2-10-2:



2.11 Size Dimension

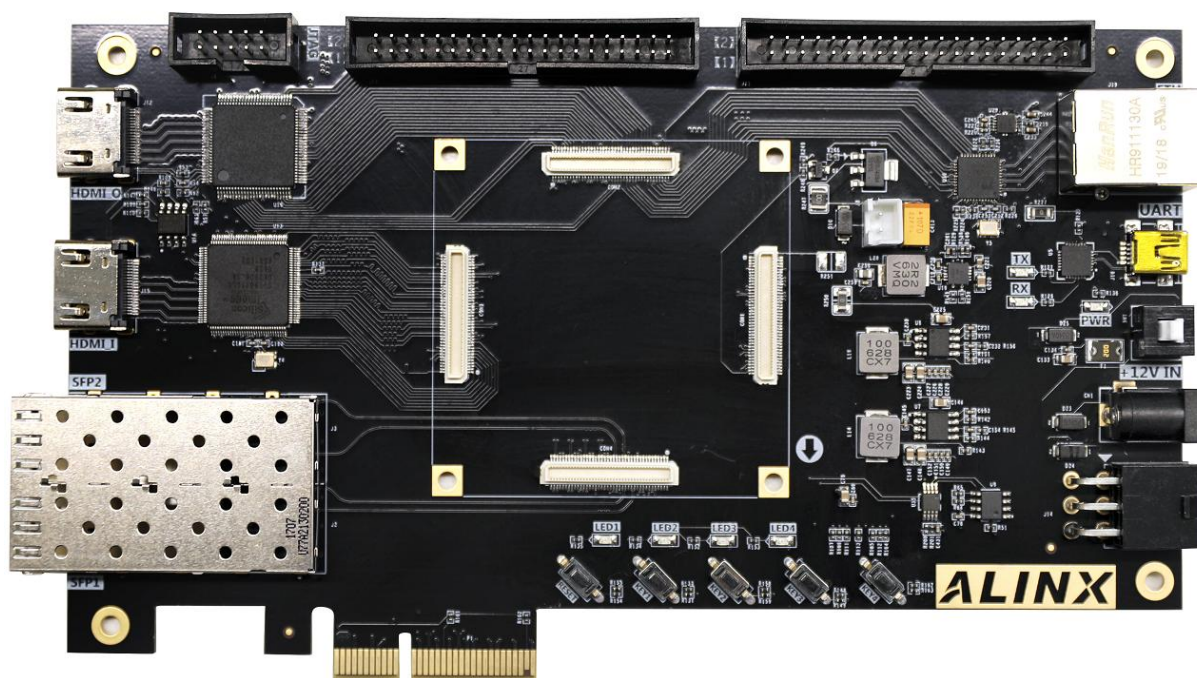


Front View



Back View

3. Carrier Board



3.1 Introduction

Through the previous function introduction, you can understand the function of the carrier board:

- 1-channel PCIe x2 high-speed data transmission interface
- 2-channel SFP high-speed fiber interfaces
- 1-channel HDMI video input interface
- 1-channel HDMI video output interface
- 1-channel 10/100M/1000M Ethernet RJ-45 interface
- 1-channel USB-to-Uart communication interface
- 1-channel SD card interface
- 2-channel 40-pin expansion ports
- EEPROM
- JTAG debugging interface
- 5 independent keys
- 4 user LED lights

3.2 Gigabit Ethernet Interface

The AX7A035B development board provides network communication services for users through a JL2121-N040I Ethernet PHY chip from JLSemi company. The Ethernet PHY chip is connected to the IO interface of the ARTIX7 FPGA. The JL2121-N040I chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. JL2121-N040I supports MDI/MDX self-adaptive, various speed self-adaptive, Master/Slave self-adaptive, supports MDIO bus for PHY register management.

When the JL2121 is powered on, it detects some specific IO level states to determine its own working mode. Table 3-2-1 describes the default Settings of the GPHY chip after it is powered on.

Configuration Pin	Instructions	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

表 3-2-1PHY 芯片默认配置值

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through the RMII bus, the transmission clock is 25Mhz, and the data is sampled on the rising and falling edge of the clock.

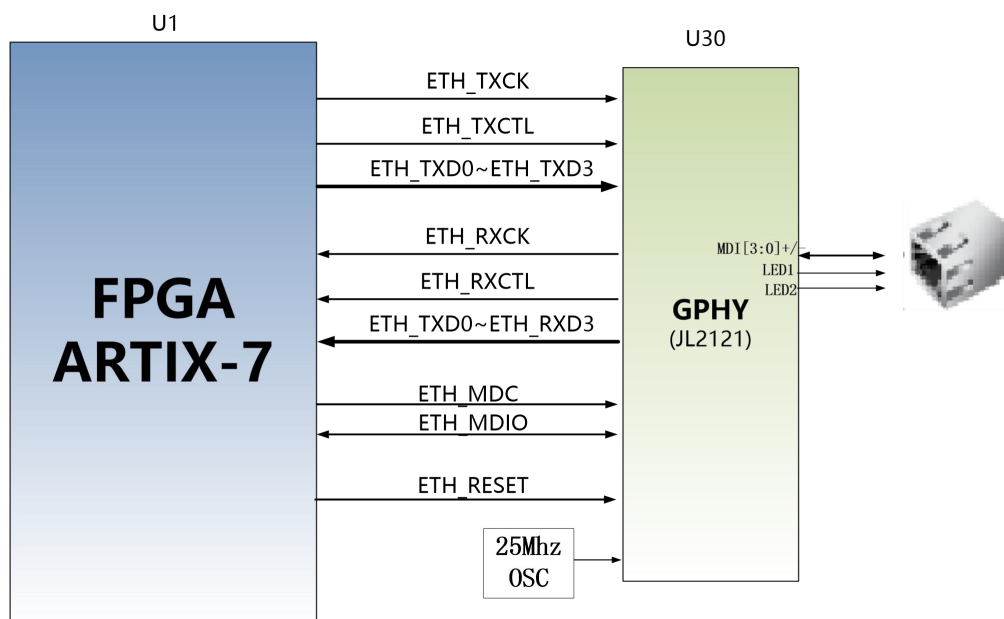


Figure 3-2-1: connection diagram between FPGA and Ethernet PHY chip

Ethernet PHY FPGA pin assignment:

Signal Name	FPGA Pin Number	Description
ETH_TXCK	P15	RGMII sends the clock
ETH_TXD0	N14	Send data bit0
ETH_TXD1	P16	Send data bit1
ETH_TXD2	R17	Send data bit2
ETH_TXD3	R16	Send data bit3
ETH_TXCTL	N17	Send the enable signal
ETH_RXCK	V18	RGMII receives the clock
ETH_RXD0	P19	Receive data Bit0
ETH_RXD1	U18	Receive data Bit1
ETH_RXD2	U17	Receive data Bit2
ETH_RXD3	P17	Receive data Bit3
ETH_RXCTL	R19	Receive data valid signal
ETH_MDC	N13	MDIO manages the clock
ETH_MDIO	P14	MDIO manages the data
ETH_RESET	R14	PHY chip reset

3.3 SFP Interface

The AX7A035B FPGA development board has two optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G optical modules on the market) and insert them into these two optical interfaces for optical data communication. The two fiber interfaces are respectively connected to the two RX/TX of FPGA GTP transceiver. The TX signal and the RX signal are connected to the FPGA and the optical module through the straight separation capacitor in differential signal mode, and the data rate of each TX transmit and RX receive is up to 6.6Gb/s. The reference clock for the GTP transceiver is provided by the 125Mhz differential clock of AC7A035 FPGA core board.

Figure 3-3-1 shows the schematic diagram of FPGA and optical fiber design:

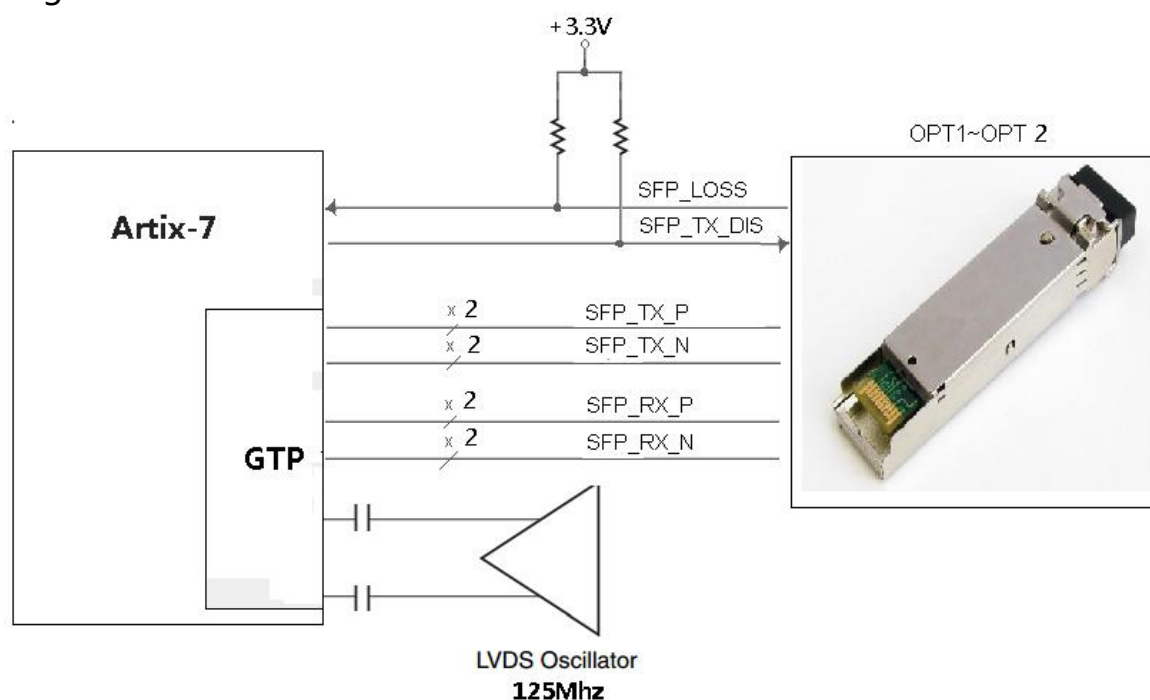


Figure 3-3-1: SFP Interface Schematic

The 1st fiber interface FPGA pin assignment:

Signal Name	FPGA Pin	Description
SFP1_TX_P	B4	SFP optical module data transmission Positive
SFP1_TX_N	A4	SFP optical module data transmission Negative
SFP1_RX_P	B8	SFP optical module data reception Positive
SFP1_RX_P	A8	SFP optical module data reception Negative

SFP1_TX_DIS	J15	SFP optical module optical emission prohibition, high efficiency
SFP1_LOSS	H15	SFP optical receive LOSS signal, High level means no light signal is received

The 2nd fiber interface FPGA pin assignment:

Signal Name	FPGA Pin	Description
SFP2_TX_P	D5	SFP optical module data transmission Positive
SFP2_TX_N	C5	SFP optical module data transmission Negative
SFP2_RX_P	D11	SFP optical module data reception Positive
SFP2_RX_P	C11	SFP optical module data reception Negative
SFP2_TX_DIS	H14	FP optical module optical emission prohibition, high efficiency
SFP2_LOSS	J14	SFP1 optical receive LOSS signal, High level means no light signal is received

3.4 PCIe x4 Interface

The AX7A035B carrier board provides an industrial-grade high-speed data transmission PCIe x2 interface. The PCIE card dimensions meet the electrical requirements of standard PCIe cards, and can be used directly in the x2 PCIe slot of a common PC.

The receiving and sending signals of the PCIe interface are directly connected to the GTP transceiver of the FPGA, and the four-channel TX signal and RX signal are connected to the FPGA by differential signal mode, and the single-channel communication rate can be as high as 5G bit bandwidth. The PCIe reference clock is provided to the development board by the PCIe slot on the PC. The reference clock frequency is 100Mhz.

The design diagram of the PCIe interface of the development board is shown in Figure 3-4-1, where the TX sending signal and the reference clock CLK signal are connected in AC coupling mode.

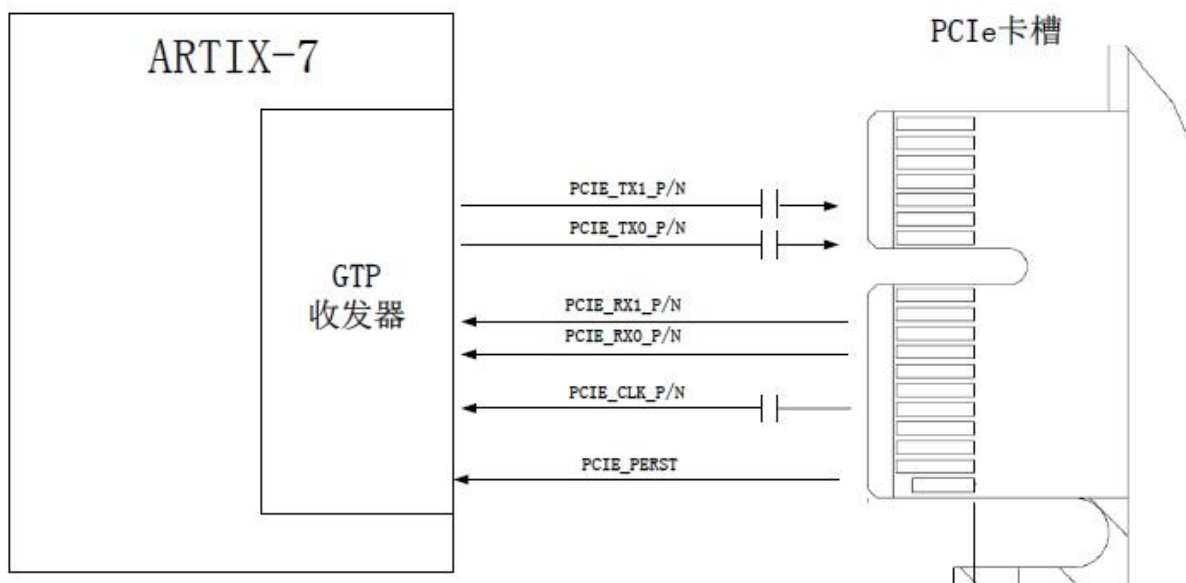


Figure 3-4-1: PCIe x2 design diagram

PClex2 Interface Pin Assignment:

Signal Name	FPGA Pin	Description
PCIE_RX0_P	D9	PCIE channel 0 data reception Positive
PCIE_RX0_N	C9	PCIE channel 0 data reception Negative
PCIE_RX1_P	B10	PCIE channel 1 data reception Positive
PCIE_RX1_N	A10	PCIE channel 1 data reception Negative
PCIE_TX0_P	D7	PCIE channel 0 data transmission Positive
PCIE_TX0_N	C7	PCIE channel 0 data transmission Negative
PCIE_TX1_P	B6	PCIE channel 1 data transmission Positive
PCIE_TX1_N	A6	PCIE channel 1 data transmission Negative
PCIE_CLK_P	F10	PCIE Reference Clock Positive
PCIE_CLK_N	E10	PCIE Reference Clock Negative

3.5 HDMI Output Interface

The HDMI output interface is implemented by using Silion Image's SIL9134 HDMI (DVI) coding chip, which supports the highest 1080P@60Hz output and 3D output.

Among them, the IIC configuration interface of SIL9134 is also connected

to the IO of FPGA, and initialization and control operations are performed on SiI9134 through FPGA programming. The hardware connection of the HDMI output interface is shown in Figure 3-5-1.

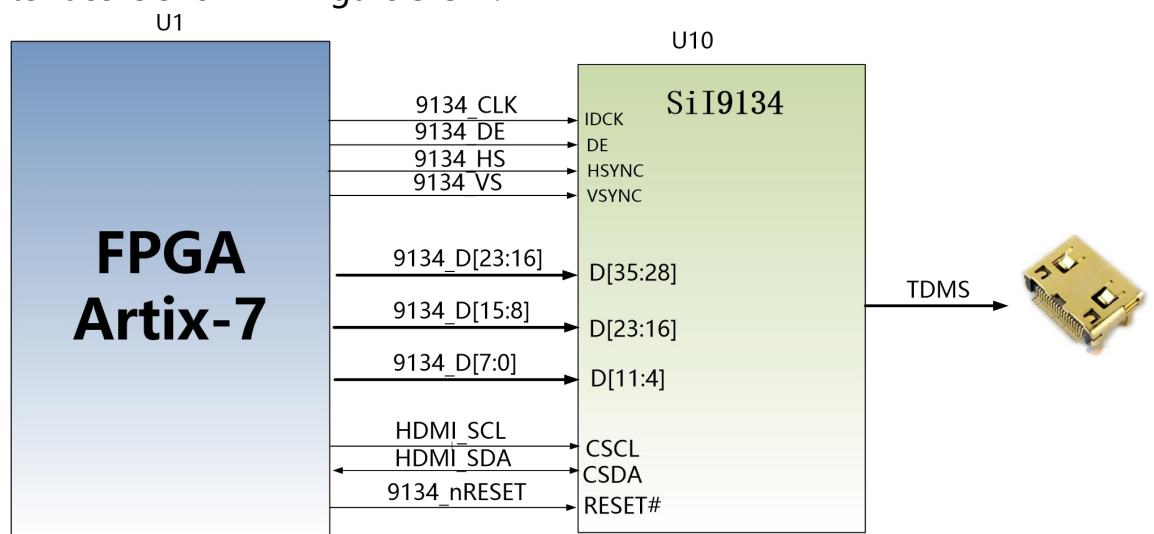


图 3-5-1 HDMI 接口设计原理图

HDMI Input Pin Assignment:

Pin Name	FPGA Pin
9134_NRESET	L18
9134_CLK	Y22
9134_HS	T18
9134_VS	R18
9134_DE	U22
9134_D0	V22
9134_D1	Y18
9134_D2	Y19
9134_D3	W19
9134_D4	W20
9134_D5	Y21
9134_D6	U21
9134_D7	T21
9134_D8	W21
9134_D9	W22
9134_D10	T20

9134_D11	AB18
9134_D12	AA18
9134_D13	AA19
9134_D14	AB20
9134_D15	AA20
9134_D16	AA21
9134_D17	AB22
9134_D18	AB21
9134_D19	W17
9134_D20	V17
9134_D21	V20
9134_D22	U20
9134_D23	V19
HDMI_SCL	H13
HDMI_SDA	G13

3.6 HDMI Output Interface

We use Silion Image's SIL9013 HDMI decoding chip, which supports the highest 1080P@60Hz input and supports data output in different formats.

Among them, the IIC configuration interface of SIL9013 is also connected to the IO of FPGA, and initialization and control operations are carried out on SIL9013 through FPGA programming. The hardware connection of the HDMI input interface is shown in Figure 3-6-1.

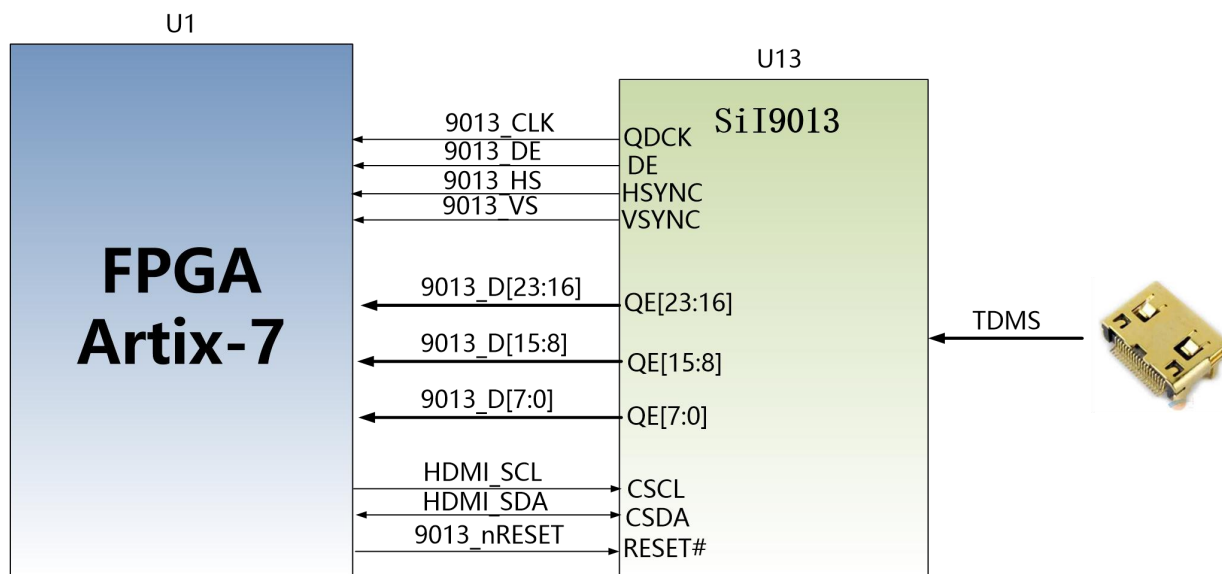


Figure 3-6-1: HDMI input schematic

HDMI Input Pin Assignment:

Pin Name	FPGA Pin
9013_NRESET	J21
9013_CLK	K18
9013_HS	N18
9013_VS	M18
9013_DE	N19
9013_D0	M20
9013_D1	N20
9013_D2	L21
9013_D3	M21
9013_D4	K19
9013_D5	H17
9013_D6	H18
9013_D7	N22
9013_D8	M22
9013_D9	K22
9013_D10	K21
9013_D11	J22

9013_D12	H22
9013_D13	H20
9013_D14	G20
9013_D15	M17
9013_D16	J16
9013_D17	G17
9013_D18	G18
9013_D19	G15
9013_D20	G16
9013_D21	J19
9013_D22	H19
9013_D23	J20
HDMI_SCL	H13
HDMI_SDA	G13

3.7 SD Card Slot

SD Card (Secure Digital Memory Card) is a memory card based on semiconductor flash memory process, and this concept was led by Japan's Panasonic in 1999, researched and developed by Toshiba and the United States SanDisk company. In 2000, these companies launched the Secure Digital Association (SDA), which attracted a large number of manufacturers to participate, including IBM, Microsoft, Motorola, NEC, Samsung and others. Driven by these leaders, SD cards have become the most widely used memory card in consumer digital devices.

SD card is now a very commonly used storage device, and the SD card we extended supports SPI mode and SD mode, the use of SD card. The SD card used is MicroSD card. The schematic diagram is shown in Figure 3-7-1 below.

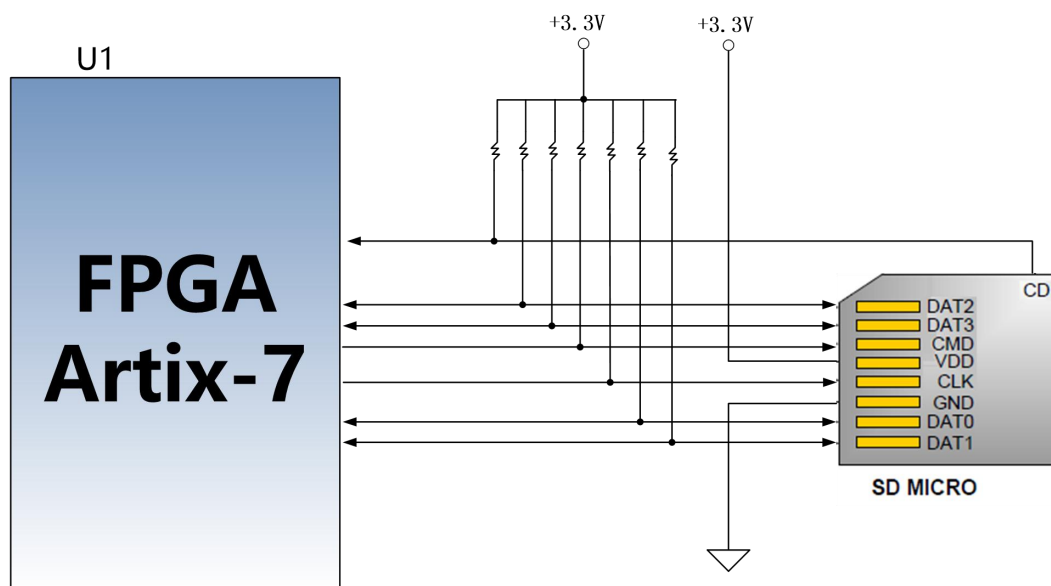


Figure 3-7-1: SD card slot schematic

SD card slot pin assignment:

SD Mode	
Pin Name	FPGA Pin
SD_CLK	E13
SD_CMD	E14
SD_CD_N	C13
SD_DAT0	D15
SD_DAT1	D14
SD_DAT2	F14
SD_DAT3	F13

3.8 USB to Serial Port

The AX7A035B development board contains the USB-UAR chip of Silicon Labs CP2102GM. The USB interface adopts the MINI USB interface and can be connected to the USB port of the PC with a USB cable for serial data communication.

The schematic diagram of USB Uart circuit design is shown in the following figure:

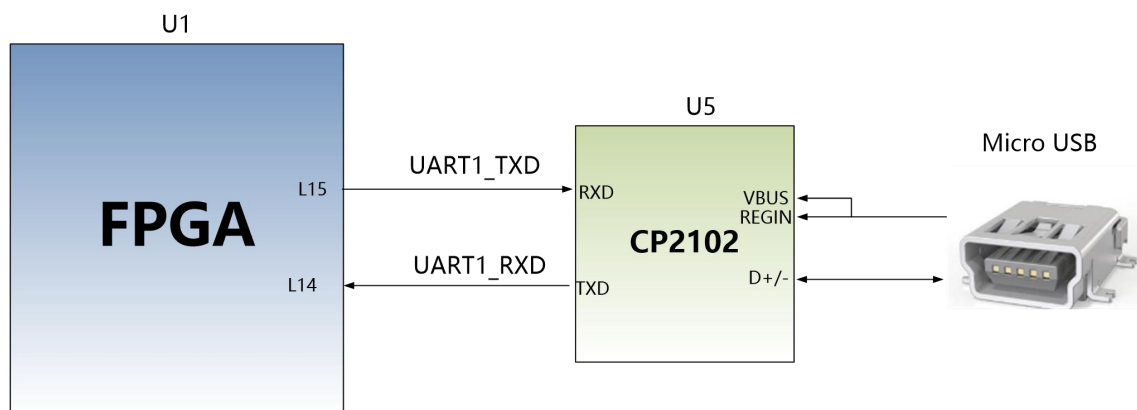


Figure 3-8-1: USB to serial port schematic

At the same time, two LED lights (LED3 and LED4) with silk-screen TX and RX on the PCB are set for the serial signal. The LED lights of TX and RX will indicate whether the serial port has data transmission or data reception, as shown in the following figure.

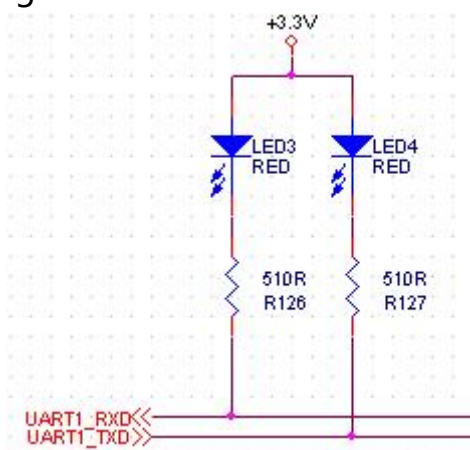


Figure 3-8-2: USB-to-serial signal indicator

FPGA pin assignment:

Pin Name	FPGA Pin
UART1_RXD	L14
UART1_TXD	L15

3.9 EEPROM 24LC04

The AX7A035B development board carries an EEPROM, model: 24LC04, capacity: 4Kbit (2*256*8bit), consists of two 256byte blocks, and communicates through the IIC bus. On-board EEPROM is to learn the communication mode of

IIC bus. The I2C signal of the EEPROM is connected to the BANK15 IO port of the FPGA end. Figure 3-9-1 shows the design diagram of EEPROM.

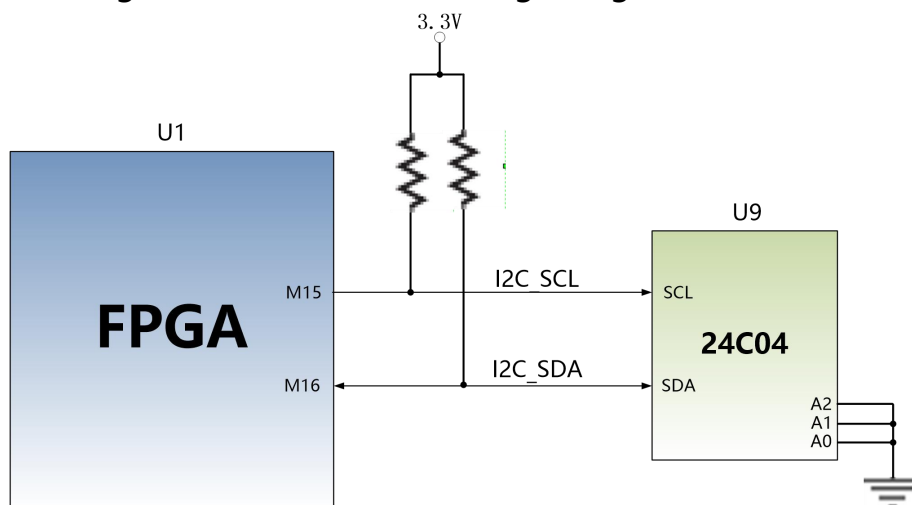


Figure 3-9-1 EEPROM schematic

EEPROM pin assignment:

Pin Name	FPGA Pin
I2C_SCL	M15
I2C_SDA	M16

3.10 Temperature Sensor

The AX7A035B development board is equipped with a high-precision, low-power, digital temperature sensor chip, model LM75, from ON Semiconductor. The temperature accuracy of LM75 chip is 0.5 degrees, and the sensor and FPGA are I2C digital interface, and the FPGA reads the temperature near the current development board through the I2C interface. Figure 3-10-1 shows the design diagram of the LM75 sensor chip.

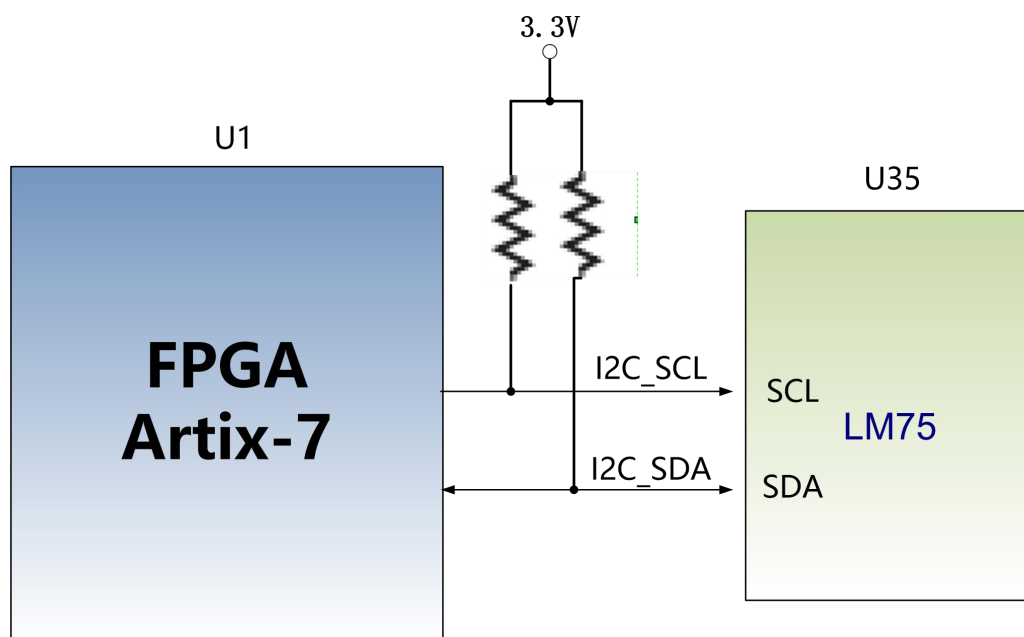


Figure 3-10-1 LM75 sensor schematic

LM75 sensor Pin Assignment:

Pin Name	FPGA Pin
I2C_SCL	M15
I2C_SDA	M16

3.11 Expansion Ports

The expansion board reserves two 2.54mm standard pitch 40-pin expansion ports J11 and J13 (**J13 is not available for AX7A035B**), which are used to connect ALINX modules or the external circuit designed by the user himself. The expansion ports have 40 signals, including 1-channel 5V power supply, 2-channel 3.3V power supplies, 3-channel ground supplies, and 34 IO ports. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The circuit of the expansion port (J11) is shown in Figure 3-11-1:

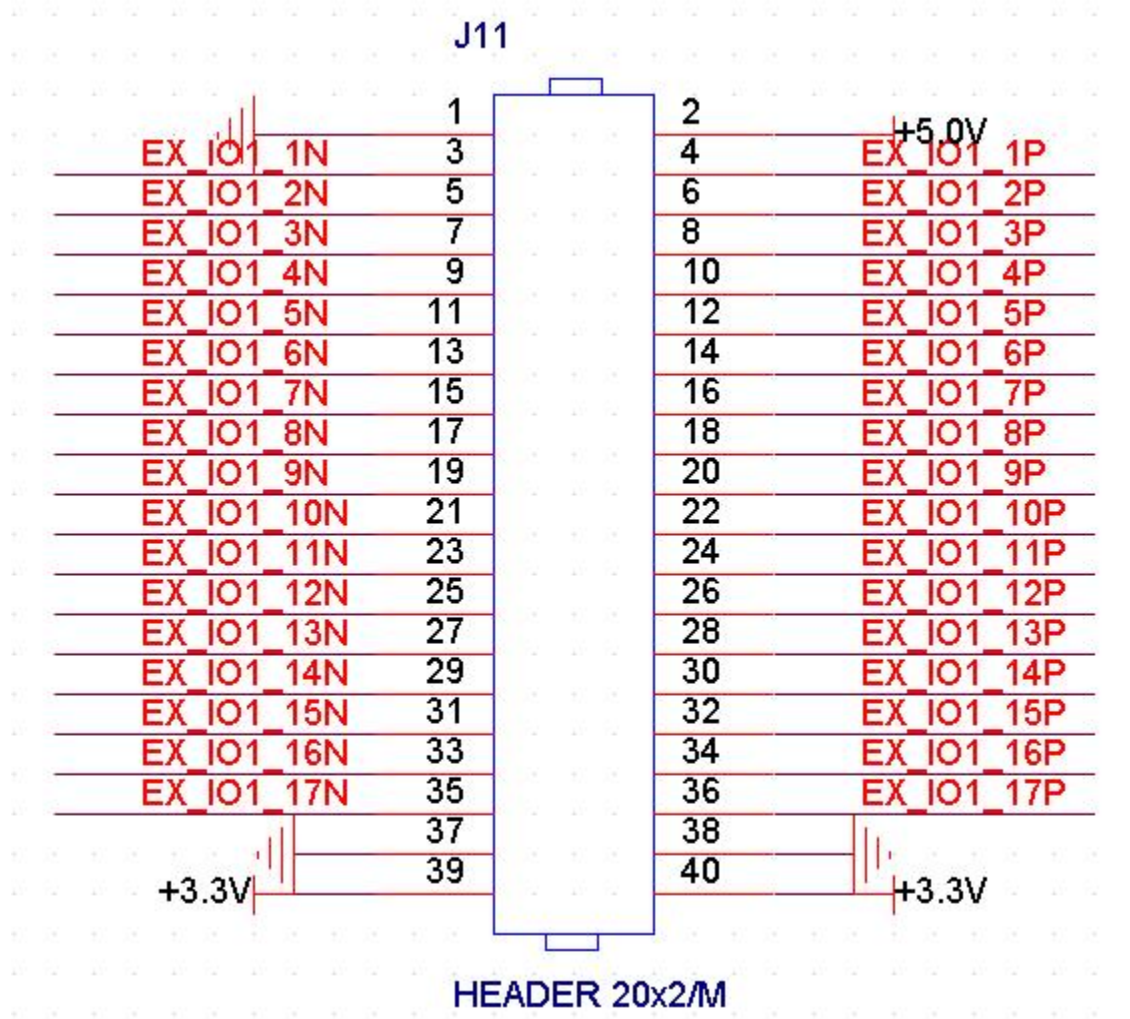


Figure 3-11-1: J11 schematic

J11 FPGA pin assignment:

No.	FPGA Pin	No.	FPGA Pin
1	GND	2	+5V
3	G21	4	G22
5	C22	6	B22
7	F19	8	F20
9	D20	10	C20
11	A18	12	A19
13	B20	14	A20
15	F18	16	E18
17	E19	18	D19

19	C18	20	C19
21	B17	22	B18
23	D17	24	C17
25	A15	26	A16
27	B15	28	B16
29	A13	30	A14
31	E16	32	D16
33	C14	34	C15
35	F16	36	E17
37	GND	38	GND
39	+3.3V	40	+3.3V

The circuit of the expansion port (J13) is shown in Figure 3-11-2 below:

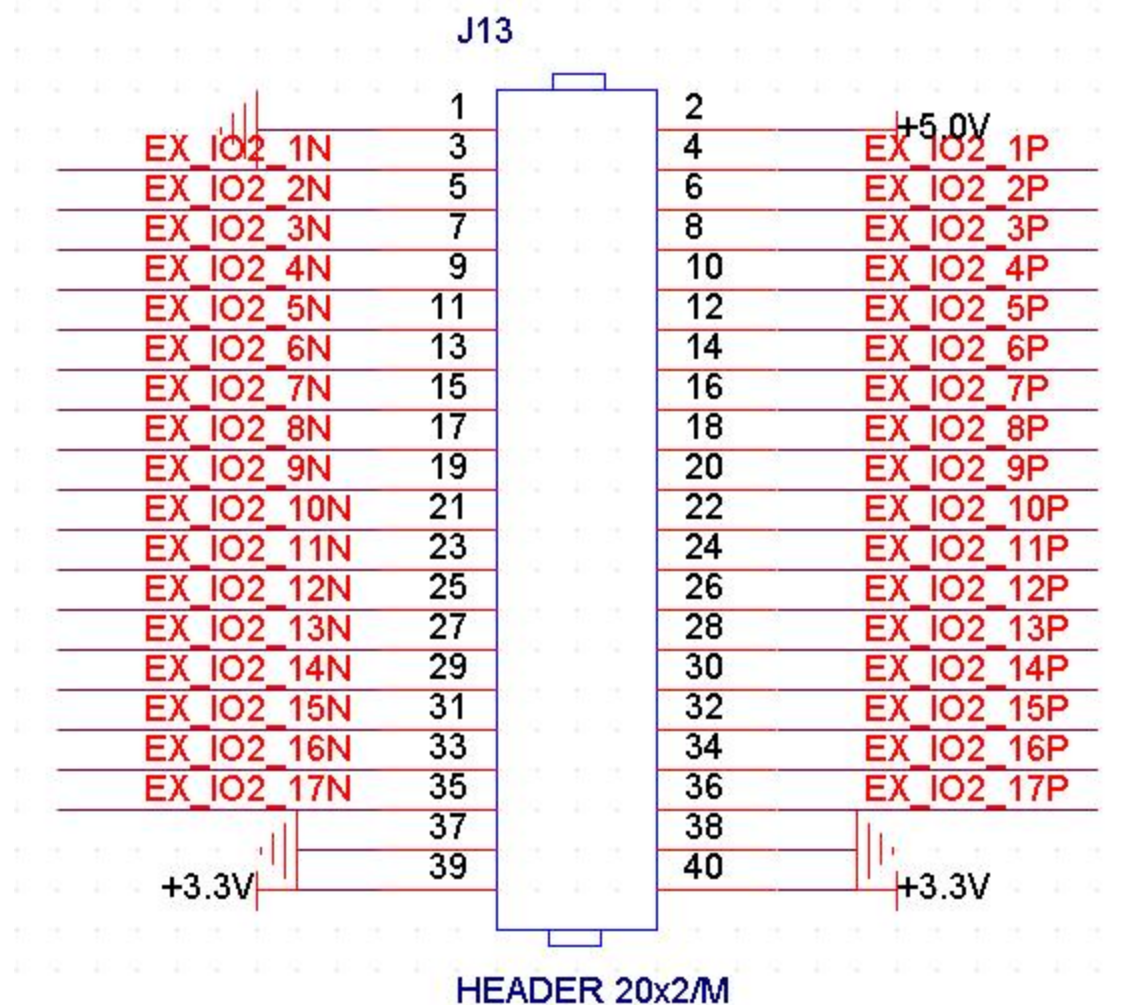


Figure 3-11-2: J13 schematic

Note: The IO of J13 is connected to BANK13, so the J13 expansion port on the AX7A035B development board is unavailable.

J13 FPGA pin assignment:

No.	FPGA Pin	No.	FPGA Pin
1	GND	2	+5V
3	W16	4	W15
5	T15	6	T14
7	V15	8	U15
9	V14	10	V13
11	W12	12	W11
13	Y12	14	Y11
15	W10	16	V10
17	AA10	18	AA11
19	AA9	20	AB10
21	U16	22	T16
23	AA13	24	AB13
25	AB11	26	AB12
27	Y13	28	AA14
29	W14	30	Y14
31	Y16	32	AA16
33	AB16	34	AB17
35	AA15	36	AB15
37	GND	38	GND
39	+3.3V	40	+3.3V

3.12 JTAG Interface

The development board reserves a JTAG interface for downloading FPGA programs or curing programs to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, we add a protection diode to the JTAG signal to ensure that the signal voltage is in the range accepted by the FPGA, so

as to avoid the damage to the FPGA.

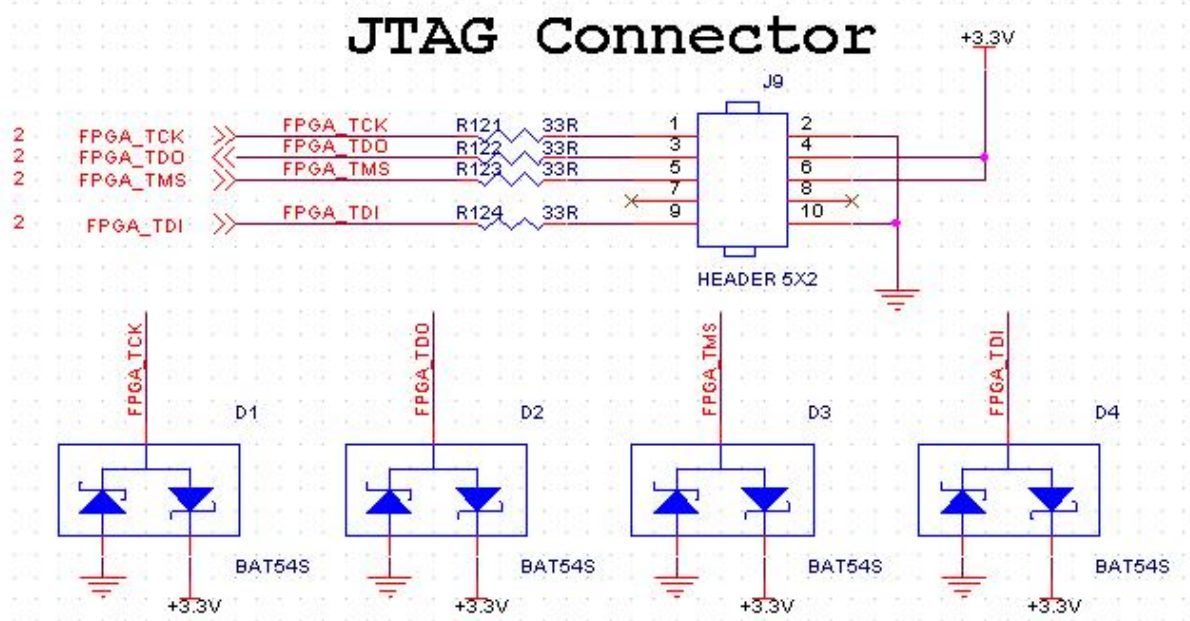


Figure 3-12-1: JTAG interface schematic

3.13 Keys

The carrier board contains five user keys: RESET and KEY1 to KEY4, which are connected to the normal IO of the FPGA. The key is valid at low level. When the key is pressed, the FPGA IO input voltage is low; when no key is pressed, the FPGA IO input voltage is high. The key circuit is shown in Figure 3-13-1 below:

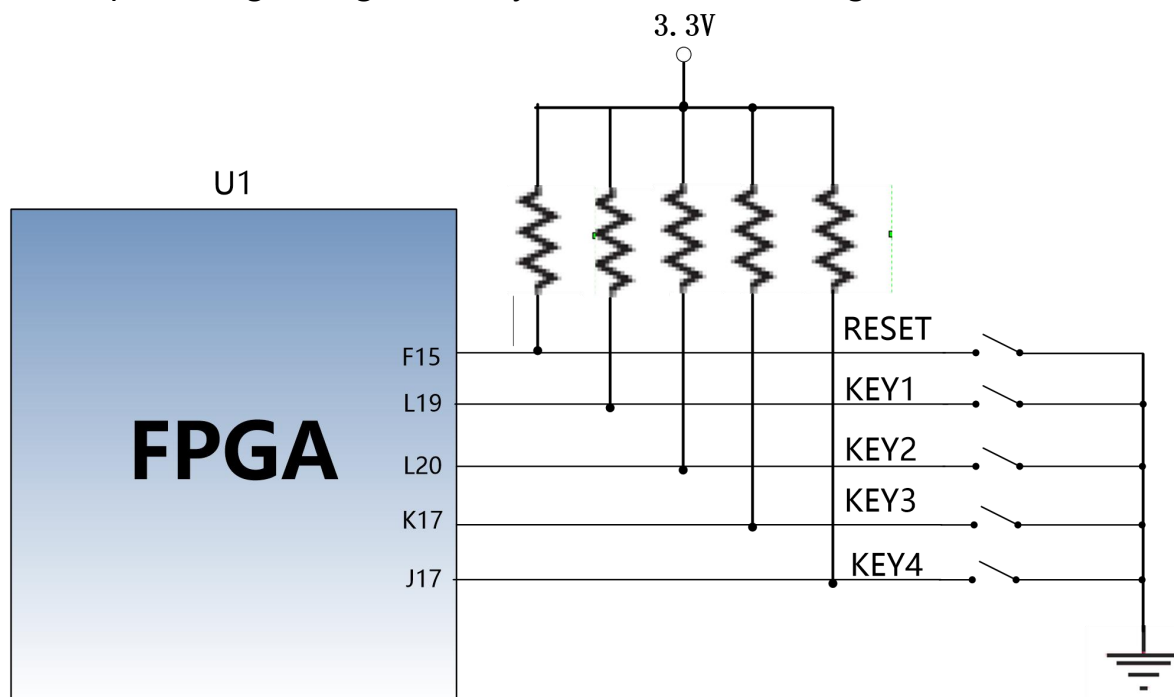


Figure 3-13-1: key Schematic

keys pin assignment:

Pin Name	FPGA Pin
RESET	F15
KEY1	L19
KEY2	L20
KEY3	K17
KEY4	J17

3.14 LED Light

There are 7 red LEDs on the AX7A035B FPGA carrier board, one of which is the power indicator (PWR), two are USB Uart data receiving and transmitting indicators, and four are users LED lights (LED1~LED4). When the board is powered on, the power indicator will light up; User LED1~LED4 are connected to the normal IO of the FPGA. When the IO voltage connected to the user LED is configured as low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be off. The schematic diagram of the user LEDs hardware connection is shown in Figure 3-14-1:

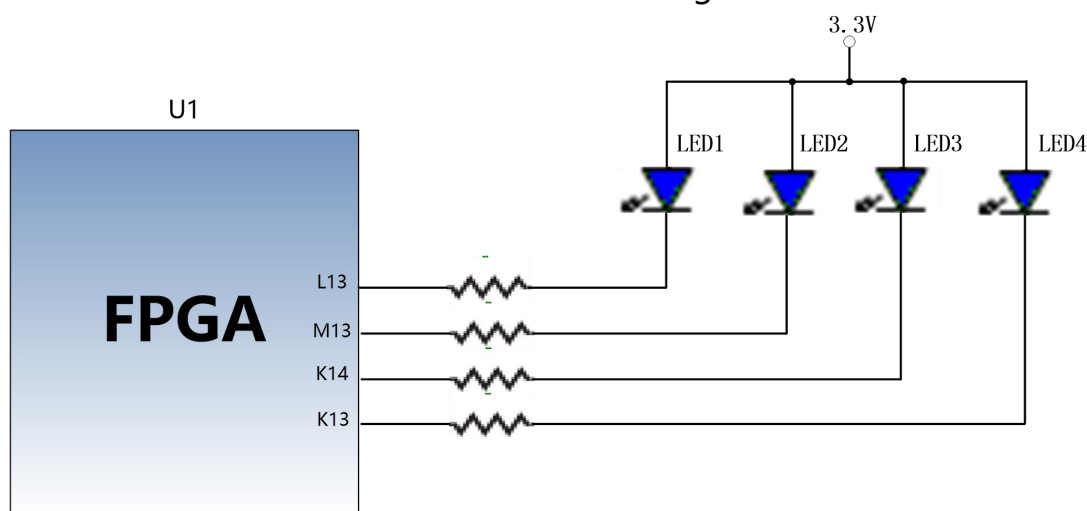


Figure 3-14-1 LED hardware design

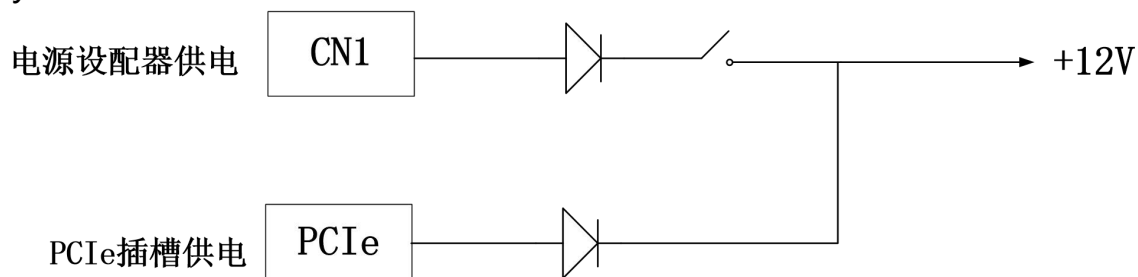
FPGA pin assignment:

Pin Name	FPGA Pin
----------	----------

LED1	L13
LED2	M13
LED3	K14
LED4	K13

3.15 Power Supply

The power input voltage of the development board is DC12V, please use the power supply of the development board, do not use power supplies with other specifications, so as to avoid damage to the development board. The development board can also obtain power from the PCIe port or the 12V power supply in the ATX chassis.



The +12V voltage is converted to +5V, +3.3V and +1.8V by three DC/DC power chips on the carrier board. The power supply design on the carrier board is shown in Figure 3-15-1 below:

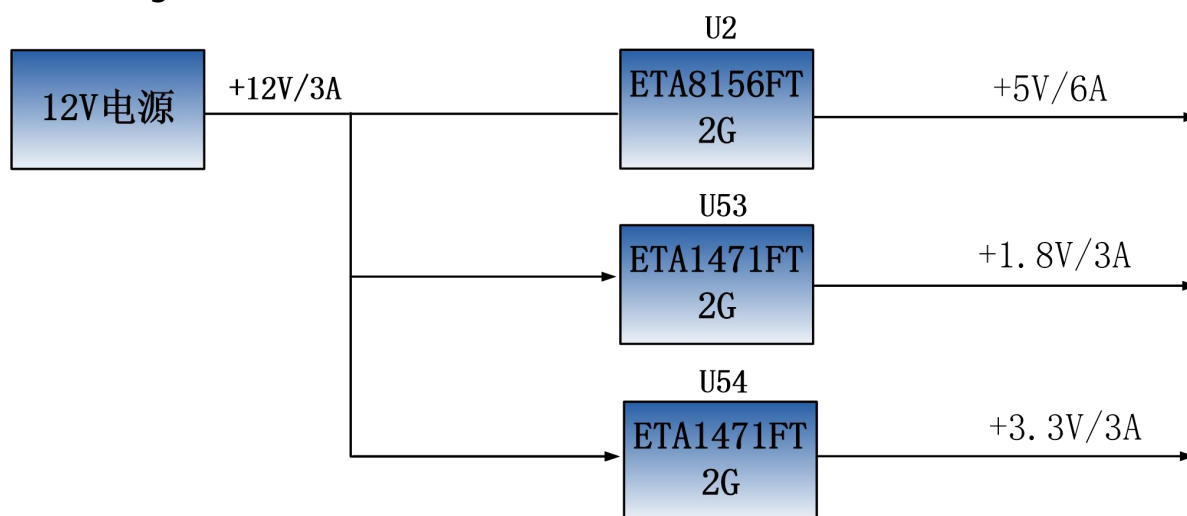


Figure 3-15-1: Power supply schematic

3.16 Fan Interface (Reserved)

Because the FPGA chip generates heat during normal operation, we reserve a fan interface on the board (the fan is not installed). The control of the fan is controlled by the FPGA chip, and the control pin is connected to the IO of the BANK16. If the IO level output is low, the MOSFET tube will be on and the fan will work. If the IO level output is high, the fan will stop. The fan design drawing on the board is shown in Figure 3-16-1 below:

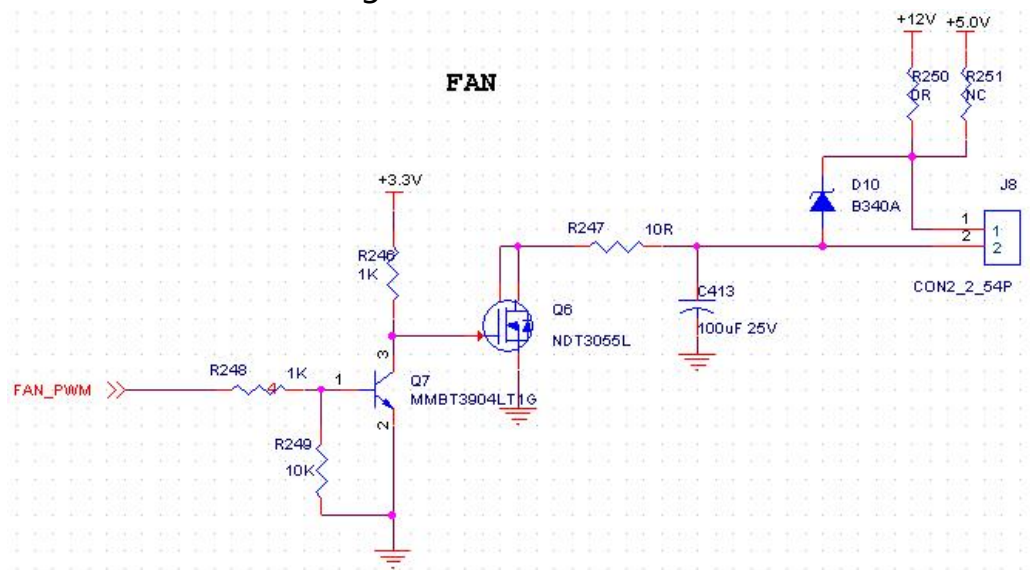
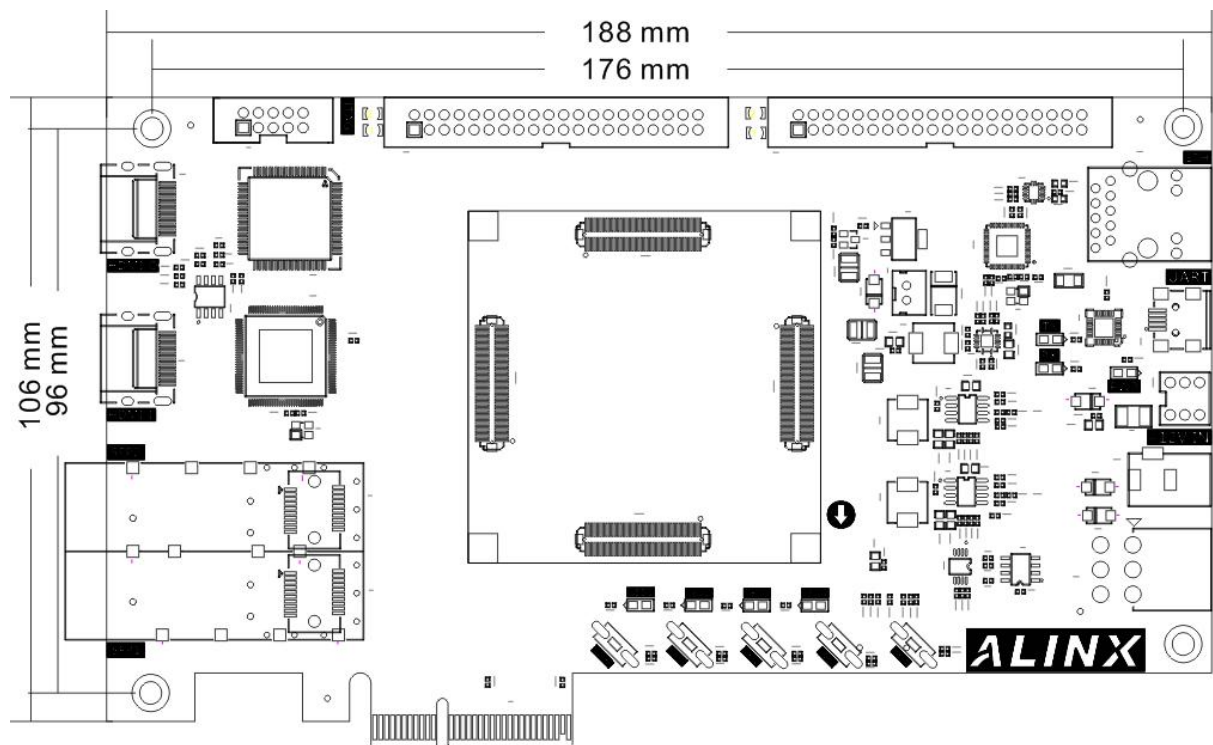


Figure 3-16-1 Fan design schematic

The fan has been fixed on the development board with screws before leaving the factory. The power supply of the fan is connected to the socket of the J8. The red one is positive and the black one is negative.

3.17 Size Dimension



Top View